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Implementation of Multimode Interleaver Address Generator for Wireless Application

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Abstract

In this brief the Low-complexity and novel technique is developed to implement efficiently the address generation circuitry of the interleaver used in the WiMAX and WLAN transreceiver. Wireless communication is one of the most vibrant research areas in the communication field. WLAN and WiMAX are emerging standards for wireless broadband communication system. The OFDM multiplexing technique used in above standards for reducing the inter symbol interference over wireless channel. The various modulation schemes such as Binary phase shift keying (BPSK), quadrature phase shift keying (QPSK), 16-quadrature amplitude modulation (QAM) and 64-QAM can be used to generate the address in interleaver structure. The channel interleaver employed in the communication system for minimizing the effect of burst error and improving the performance of FEC codes in wireless channel. The complex mathematical formulas can be replaced with optimized hardware structures. The modified structure to be used for both applications. Due to this compact structure the circuit complexity and area can be reduced. The structure can be implemented in FPGA using VHDL coding.

Keywords: OFDM, FEC, FPGA, WLAN, WiMAX, VHDL..

Introduction

The main function of a communication system is to transmit information from source to destination with sufficient reliability. The error correction codes (ECC) play very important role in modern digital communication systems. High processing speed, design flexibility and fast design Turnaround Time (TAT) is the important requirements of BWA. These requirements make the designers to choose reconfigurable hardware platform like Field Programmable Gate Array (FPGA). FPGA is an emerging technology to implement wireless standards like WLAN and WiMAX. The FPGAs offer high flexibility which means that many functions can be placed on the most efficient location in the logic flow of the device rather than in peripheral hardware. A product implemented on FPGA can easily be upgraded by making necessary changes in the Hardware Description Language (HDL) code. Broadband wireless access (BWA) provides enhancement in multimedia data services and quality of service (QoS). It support simultaneous voice, data and multimedia services to a large group of subscribers without the need for digital subscriber line (DSL) or cable modem. WLAN and WiMAX are emerging standards for wireless broadband communication system. Orthogonal frequency division multiplexing (OFDM) is a multiplexing technique used in above standards. OFDM has grown dramatically in the field of wireless communication because of its robustness against multipath delay spread. In OFDM the high rate data stream (bandwidth *W*) is decomposed into *N* lower rate data streams and then they are transmitted simultaneously over a large number of subcarriers [2]. The overlapping of subcarriers is allowed because the orthogonality ensures the separation of subcarriers at the receiver end. This approach results in a better spectral efficiency than that of FDMA systems where no spectral overlap of carriers is allowed.

WiMAX is an emerging standard for wireless broadband networking. It is based on wireless metropolitan area networking (WMAN) standards. It offers a rich set of features with a lot of flexibility in terms of deployment options and potential service offerings. The WiMAX physical layer (PHY) is based on orthogonal frequency division multiplexing which offers good resistance to multipath and allows WiMAX to operate in Non-Line of Site (NLOS) conditions whereas Wireless Local Area Network (WLAN) interconnects two or more communicating devices using some wireless distribution method and

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usually providing a connection through an access point (AP) to the wider internet [4]. WLANs can be used in different user environments namely home, corporate and public environment etc. WLANs are used to connect wireless users to a fixed LAN in corporate environments. A major WLAN application used in public sectors where WLAN can be used to connect a user to the backbone network. Airports, hotels, high-rising offices, city centers will be target area for such public WLAN usage [5].

he organization of the rest of this brief is as follows: Section II explains the interleaving technique of the wireless system. In Section III, proposes the key difference between WiMAX and WLAN. The simulation result shown in Section IV. Finally, this brief is concluded with the FPGA implementation result in section V.

Interleaving in Wireless System

Interleaving is a technique that can be used in digital communications systems to enhance the error correcting capabilities of block codes. Interleaving is an important and powerful technique to combat burst of errors for FEC coded signal. This technique is traditionally used to reduce bit error rate (BER) of digital transmission over a burst channel. The interleaver subsystem rearranges the encoded symbols over multiple code blocks. This effectively spreads out long burst noise sequences so they appear to the decoder as independent random symbol errors which are manageable burst errors. The interleaver depth varies with modulation scheme. The interleaver is defined by a two-step permutation.

1) The adjacent coded bits are mapped to non-adjacent subcarriers.
2) Adjacent coded bits are mapped alternately to less and

more significant bits of the constellation to avoid long run
of lowly reliable bits.

The interleaver structure is shown in fig.1.interleaver consists of two sections: address generator and interleaver memory.

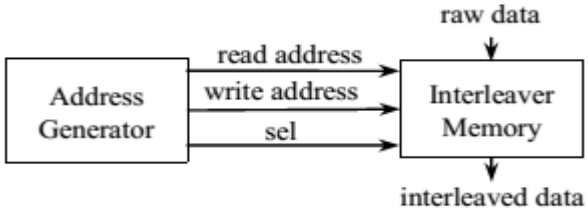

Fig. 1. Interleaver structure

The address generator is basically the simultaneous implementation of (1) and (2) which is the write address along with provision for generation of read address for interleaver memory. Block interleaver uses two memory blocks out of which one memory block is written and the other is read based on the value of select (sel) signal. Interleaving is frequently used in digital communication to improve the performance of forward error correcting codes. Many communication channels are not memory less: errors typically occur in bursts rather than independently. If the number of errors within a code word exceeds the error-correcting code's capability, it fails to recover the original code word. Interleaving ameliorates this problem by shuffling source symbols across several code words, thereby creating a more uniform distribution of errors. Therefore, interleaving is widely used for burst error correction.

A. FORWARD ERROR CORRECTION CODE

In telecommunication, information theory, and coding theory, forward error correction (FEC) or channel coding is a technique used for controlling errors in data transmission over unreliable or noisy communication channels. The central idea is the sender encodes their message in a redundant way by using an error-correcting code (ECC).The redundancy allows the receiver to detect a limited number of errors that may occur anywhere in the message, and often to correct these errors without retransmission. FEC gives the receiver the ability to correct errors without needing a reverse channel to request retransmission of data. FEC is therefore applied in situations where retransmissions are costly or impossible, such as one-way communication links and when transmitting to multiple receivers in multicast. FEC information is usually added to mass storage devices to enable recovery of corrupted data, and is widely used in modems. FEC processing in a receiver may be applied to a digital bit stream or in the demodulation of a digitally modulated carrier. For the latter, FEC is an integral part of the initial analog-to-digital conversion in the receiver.

Many FEC coders can also generate a bit-error-rate (BER) signal which can be used as feedback to fine-tune the analog receiving electronics. The maximum fractions of errors or of missing bits that can be corrected is determined by the design of the FEC code, so different forward error correcting codes are suitable for different conditions.

B. ADDRESS GENERATOR

The address generator circuit is used to generate (1) write addresses (2) read addresses (3) sel signals. The complete circuit is shown in Fig. 2. The circuit consists of stages of multiplexers which implement equal or unequal increments for various modulation schemes as shown in Table 1. The design concept contains three levels of multiplexer (MUX).

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The design concept contains three multiplexers (muxs): mux-1 and mux-2 implements the unequal increments required in 16-QAM and 64-QAM whereas mux-3 routes the outputs received from mux-1 and mux-2 along with equal increments of BPSK and QPSK. The select input of mux-1 is driven by a T-flip-flop named qam16_sel whereas that of mux-2 is controlled by a mod-3 counter, qam64_sel. The two lines of mod type (modulation type) are used as select input of mux-3. The 6-bit output from the mux-3 acts as one input of the 9-bit
adder after zero padding. The other input of the adder comes from accumulator, which holds the previous address. After addition a new address is written in the accumulator.

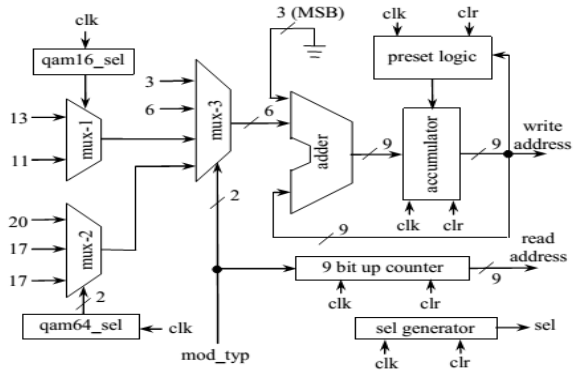

Fig. 2. Structure of address generator

The preset logic is a hierarchical FSM whose principal function is to generate the correct beginning addresses for all subsequent iterations. This block contains a 4-bit counter keeping track of end of states during the iteration. The FSM enters into the first state (SF) with clr = 1. Based on the value in mod_typ it makes transition to one of the four possible next states (SMT0, SMT1, SMT2 or SMT3). Each state in this level represents one of the possible modulation schemes. The FSM thereafter makes transition to the next level of states (e.g. S000, S001and so on) based on the value in the accumulator. When the FSM at this level reaches to the terminal value of that iteration it makes transition to a state (e.g. S000) in which it loads the accumulator with the initial value (e.g. preset=1) of the next iteration. This process continues till all the interleaver addresses are generated for the selected mod_typ. If no changes take place in the values of mod_typ, the FSM will follow the same route of transition and the same set of interleaver addresses will be continually be generated. Any change in mod_typ value causes the interleaver to follow a different path. In order to facilitate the address generator the circuit to respond to clr input followed by mod_typ inputs at any stage of the FSM. With clr=1 it comes back to SF state irrespective of its current position and there after transits to the desired states in response of new value in mod_typ. The read addresses are linear in nature and are generated using a nine bit up counter as shown in Fig. 2. The counter is reset whenever it reaches to the terminal count for a desired modulation scheme. The sel generator is basically a T-flip-flop used to generate the select (sel) signal and is initialized to zero using clr input.

Table I Interleaver Write Address For Modulation Schemes

N_{cbps}=48 bits, BPSK (mod_typ =00)	0	3	6	9	12	15	18	21
	24	27	30	33	36	39	42	45
	1	4	7	10	13	16	19	22
	25	28	31	34	37	40	43	46
N_{cbps}=96 bits, QPSK (mod_typ =01)	0	6	12	18	24	30	36	42
	48	54	60	66	72	78	84	90
	1	7	13	19	25	31	37	43
	49	55	61	67	73	79	85	91
N_{cbps}=192 bits, 16-QAM (mod_typ =10)	0	13	24	37	48	61	72	85
	96	109	120	133	144	157	168	181
	1	12	25	36	49	60	73	84
	97	108	121	132	145	156	169	180
N_{cbps}=288 bits, 64-QAM (mod_typ =11)	0	20	37	54	74	91	108	128
	145	162	182	199	216	236	253	270
	1	18	38	55	72	92	109	126
	146	163	180	200	217	234	254	271

C. INTERLEAVER MEMORY OPERATION

The structure of interleaver memory is shown in fig 3.The function of interleaver memory is as follows the interleaver memory block comprises of two memory modules (RAM-1 and RAM-2), three muxs and an inverter as shown in Fig.3. In block interleaving when one memory block is being written the other one is read and vice-versa. Each memory module receives either write address or read address with the help of the mux connected to their address inputs (A) and sel line. RAM-1 at the beginning receives the read address and RAM-2 gets the write address with write enable (WE) signal of RAM-2 active. After a particular memory block is read / written up to the desired location, the status of sel changes and the operation is reversed. The mux at the output of the memory modules routes the interleaved data stream from the read memory block to the output.

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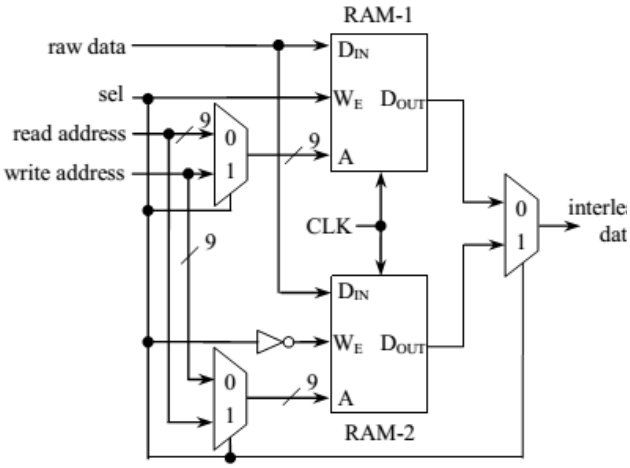

Fig. 3. Schematic diagram of interleaver memory

WIMAX Vs WLAN

Wireless Local Area Network, also known as WLAN or Wi-Fi, is the alternative to cabled LAN. It provides users mobility to move from one location to another without thinking about the wires. It has grown in popularity along with the rise of laptop computers and low cost netbooks that made mobile computing within reach for most people. WiMax stands for worldwide interoperabiliy for Microwave Access and it provides high speed internet access to areas the WLAN cannot reach. WiMax is a new technology that is still not very popular but is gaining widespread attention due to the niche it serves. WiMax equipment provides services that are in between high speed, low range WLAN and low speed, high range 3G and 2G technologies. WLAN can provide high speeds since its hardware is not meant to transmit or receive signals from far away and it does not have to deal with the substantial attenuation that comes with long distances. The 50km range of WiMax and its superior ability to pass through obstructions makes it ideal for certain applications as a last mile connectivity replacement to cables for DSL lines. The speed that can be achieved with WiMax isn't constant though, it is conversely proportional to the distance between the base station and the subscriber.

The two technologies also differ in the type of Media Access Controller or MAC that they utilize. Wi-Fi uses one that is contention based. This means that all clients who use the same access point are competing for bandwidth with the closest user getting the highest priority. WiMax uses a MAC with a scheduling algorithm that ensures each client gets assigned a certain time span to communicate with the access point. The time span allocated to each client can be reduced or expanded depending on the needs of the client but it cannot be used by other clients as long as he remains connected. Some key differences between WLANs and WMANs supported by Wi-Fi and WiMAX products:

- It's possible to use WMAN technology indoors, but 802.16 protocols are optimized for outdoor operation. It's possible to use WLAN technology outside, but 802.11 protocols were primarily designed for indoor networks.
- Larger WLANs can be constructed using many densely-spaced Wi-Fi APs, but to blanket miles of territory with wireless, you really want to create a WMAN technology.
- On the other hand, using WiMAX products for communication between PCs inside the same building would be pricey and impractical -- that's precisely what WLAN technologies were created for.
- Most office and home WLANs are composed of Wi-Fi products operating in unlicensed spectrum -- channels freely available for use by anyone. WiMAX products most often operate in spectrum licensed to wireless carriers who use them to deliver commercial BWA services.

Simulation Result

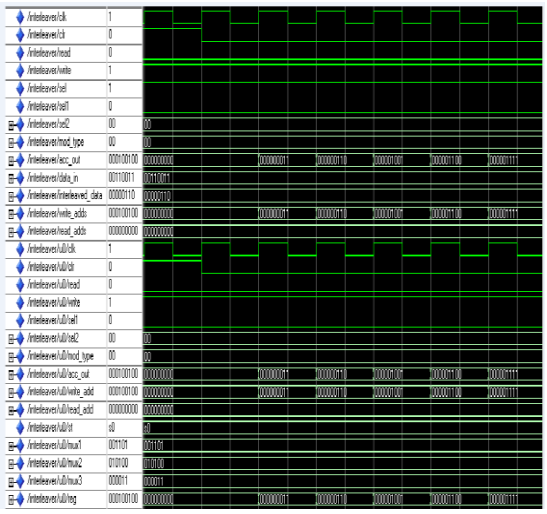

Fig. 4. Simulation result for address generator

In BPSK modulation scheme (mod_typ=00) have been chosen where first 16bits of raw data input (data_in) are held high. The effect of interleaver is visible as the consecutive 1's are dispersed by 3 bits position in the data output (data_out) line. This is because the write address sequence in BPSK modulation scheme is 0, 3, 6, 9,….47. Similar results are also obtained for other modulation schemes. The VHDL program developed for the proposed WiMAX deinterleaver address generator is downloaded on the

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Xilinx Spartan-3 (Device XC3S400) FPGA [11]. In this brief results in a significant reduction in occupancy of FPGA slices (by 80.24%), flip flops (by 35.9%), and four input LUTs (by 80.47%). This comparison clearly proves the low complexity and hardware efficiency of this design over the conventional technique. In addition, the address generator using the proposed technique can work 48.69% faster than the latter.

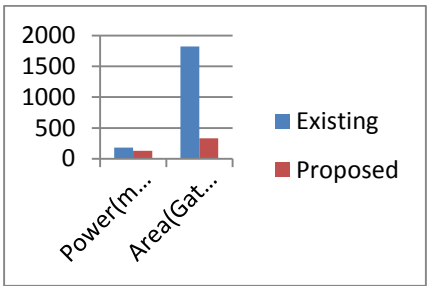

Fig.5. Area and Power Comparison

Conclusion

The address generation circuitry of the WiMax and WLAN channel deinterleaver supporting all possible code rates and modulation patterns as per IEEE802.16e and 802.11a/g/n. The VHDL coding has been developed to evaluate the area utilization. The conventional Look Up Table (LUT) based method shows the minimum period as 7.283ns and the maximum frequency was 137.30MHz. in this work the minimum period of 4.953ns is obtained, which is better than the conventional method and the corresponding maximum frequency obtained is 201.898MHz. The maximum operating frequency of the address generator is improved by approximately 49% when compared with the conventional method. By eliminating the modulo function of QPSK, 16-QAM, 64-QAM techniques, a significant reduction in the area of the address generation circuit can be achieved. The area utilization of a technique can be represented in terms of number of gate counts. The conventional method required a gate count of 1,556 logic gates and in this work the gate count is reduced to 1,524 gates. The FSM based technique is to model the interleaver used in IEEE 802.11a and IEEE 802.11g based WLAN is proposed. The proposed hardware model of the interleaver is completely implemented in Spartan-3 FPGA. Two different techniques to model the required memory in the interleaver using internal resources of FPGA have been shown. Critical analysis of implementation results of both approaches have been made to ease the decision making of a system designer regarding the technique to adopt. Both techniques make efficient use of FPGA's internal resources and consume low power thereby making themselves ideal choice for battery powered wireless equipment.

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